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Paper Code : PE-EC802C VLSI Design Automation

UPID : 008383

Time Allotted : 3 Hours

Full Marks : 70

The Figures in the margin indicate full marks.

Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer any ten of the following :

[1 x 10 = 10]

- (I) What analysis we do during floor plan?
- (II) What is the need of simulation in VLSI?
- (III) What are RTL and synthesis?
- (IV) What is the meaning of combinatorial optimization problem?
- (V) What is the clock latency?
- (VI) What is signal integrity?
- (VII) What are the types of programmable devices?
- (VIII) What is keep-out margin?
- (IX) What are the complex cells in the floor plan?
- (X) What do you mean by logic synthesis?
- (XI) What is meant by computational complexity?
- (XII) What are the different types of partitioning in VLSI?

Group-B (Short Answer Type Question)

Answer any three of the following :

[5 x 3 = 15]

2. Explain Gajski's Y chart for VLSI design. [5]
3. Describe the Kernighan-Lin (K-L) algorithm. [5]
4. What is Depth-first Search algorithm? [5]
5. What are the drawbacks of the K-L algorithm ? [5]
6. What is Dijkstra's Shortest-path Algorithm? [5]

Group-C (Long Answer Type Question)

Answer any three of the following :

[15 x 3 = 45]

7. (a) What is Computational Complexity? [5]
(b) Differentiate between tractable and Intractable problems. [5]
(c) What do you mean by combinatorial optimization. [5]
8. (a) What is the Min-cut algorithm ? Describe the different types of Min-cut algorithm. [8]
(b) Explain Bellman Ford algorithm. [7]
9. (a) What does a placement algorithm try to optimize? [7]
(b) What do the terms Cut set, Cut size, and Size of a component mean? [8]
10. (a) Explain the Line probe algorithm in VLSI design automation. [8]
(b) Discuss the Maze routing algorithm in detail. [7]
11. (a) Describe the Simulated Annealing algorithm. [10]
(b) What are the advantages of this algorithm ? [5]

*** END OF PAPER ***